REMARKS

In reply to the Office Action mailed March 25, 2010, please enter the amendments set forth above and consider the following remarks. By this response, Applicants amend claim 1, 7, 9, and 11, and present new claims 14-17. No new matter has been added. Upon entry of this paper, claims 1, 3, and 5-17 will remain pending in this application.

In the Office Action, the Examiner: (i) rejected claims 1, 3, 5, 7-8, 9, and 11-12 under 35 U.S.C. 102 as anticipated by U.S. Patent 5,826,007 (Sakaki); (ii) rejected claims 6 and 10 under 35 U.S.C. 103 as unpatentable over Sakaki in view of U.S. Patent Pub 2005/0033951 (Madter); and (iii) rejected claim13 under 35 U.S.C. 103 as unpatentable over Sakaki and Madter in view of U.S. Patent 6,118,870 (Boyle). In the interest of efficiently furthering prosecution, Applicants have amended the claims as indicated above, and submit that the claims as amended are allowable for at least the reasons set forth below.

New Claims

Applicants hereby submit new claims 14-17 depending from previous independent claim 11. Support for these new claims is found in paragraphs 82-88 of the present application.

Rejections Under 35 U.S.C. 102

The Examiner rejected claims 1, 3, 5, 7-8, 9, and 11-12 under 35 U.S.C. 102 as anticipated by U.S. Patent 5,826,007 (Sakaki).

Claims 1, 3, 5, 7-8, 9, and 11-12

Claim 1 as amended recites "wherein said protection data is only modifiable so as to increase said protection level by permanently reducing access to a part of the

protected data memory portion". Therefore, as described in claim 1, access to a portion of the non-volatile memory identified as a part of the protected data memory portion is permanently reduced. Support for this is found in at least paragraphs 10-11, 45, and 82-87 of the present application.

By way of contrast, Sakaki describes use of an S1 bit and an S2 bit. The S1 bit is describes as only being modifiable to increase protection, but access to the memory is not permanently reduced. Instead, in Sakaki, after the S1 bit is set, the memory may still be accessed, but only after the data in the memory is deleted by setting of the S2 bit (See Sakaki Col. 6 lines 3-18) and cycling power. Therefore, Sakaki does not permanently reduce access to a part of the protected data memory portion, but instead only deletes the data in the memory prior to allowing access to the memory portion.

Therefore, since Sakaki does not describe all of the recitations of claim 1 as amended, Applicants respectfully submit that claim 1 is allowable over the cited art, and the rejection should be withdrawn. Additionally, claim 9 and 11 include recitations similar to those above from claim 1, and claims 3, 5, 7-8, and 12 depend from claims 1, 9, and 11. Also, new claims 14-17 depend from claim 11. As such, these claims are allowable for at least the reasons discussed above for claim 1.

Claims 7 and 14-17

Claim 7 as amended recites "at least one address_value defining an address limit from which the data stored at said memory are protected data and access to such protected data is denied". Additionally, claim 14 recites "a first set of address data associated with the set of conditional access microprocessor instructions that is readable by the microprocessor" and claim 15 recites "the method of claim 14 wherein the access to the part of the first protected data memory portion is permanently reduced by modification of the first set of address data."

By way of contrast, Sakaki only teaches a single bit operator that impacts access to the entire memory components at issue. Sakaki does not teach using an

address value to define an address limit, or modifying an address value to reduce access to a portion of the memory by the microprocessor.

Rejections Under 35 U.S.C. 103

The Examiner rejected claims 6 and 10 under 35 U.S.C. 103 as unpatentable over Sakaki in view of U.S. Patent Pub 2005/0033951 (Madter). As discussed above, claims 1, 9, and 11 are not anticipated by Sakaki. The deficiencies of Sakaki are not cured by Madter.

Madter discloses a boot method for increasing the security of a memory device. Madter does not, however, teach or suggest that protection data is only modifiable so as to increase said protection level by permanently reducing access to a part of the protected data memory portion.

Therefore, Applicants respectfully submit that claims 1, 9, and 11 as well as 6 and 10 dependent thereon are not obvious given a combination of Sakaki and Madter.

The Examiner rejected claim 13 under 35 U.S.C. 103 as unpatentable over Sakaki and Madter in view of U.S. Patent 6,118,870 (Boyle). As discussed above, claims 1, 9, and 11 are not obvious given a combination of Sakaki and Madter. The deficiencies of Sakaki and Madter are not cured by Boyle.

Boyle discloses devices and methods for compression and decompression including use of a MIPS instruction set. Boyle does not teach or suggest that protection data is only modifiable so as to increase said protection level by permanently reducing access to a part of the protected data memory portion.

Therefore, Applicants respectfully submit that claims 1, 9, and 11 as well as claim 12 dependent thereon are not obvious given a combination of Boyle, Sakaki and Madter.

Conclusory Remarks

In view of the above, it is respectfully submitted that claims 1, 3, and 5-17 are in condition for formal allowance, and early and favorable action to that end is respectfully requested.

The Examiner is encouraged to call Applicants' attorney at the number below if doing so will in any way advance prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. **07-1896**.

Respectfully submitted,

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Date: June 25, 2010

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